

### Abstract of the Disclosure

A memory system having at least one memory subsystem and using a packet protocol communicated over a command and address bus and at least one data bus. The memory subsystems are pipelined to achieve wide data paths and to support a high number of memory devices, such as dynamic random access memory devices, per data bus. The packet protocol is defined to compensate for the delay stages of the pipelined memory subsystem in order to optimize the access time of the memory devices.

10

15

20

25

"Express Mail" mailing label number: EL530191404US

Date of Deposit: November 5, 1999

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

Printed Name: Chris Hammond

Signature: Chris Hammond